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FORM PTO-1390 (REV. 9-2001) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 302-001

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 10/069987

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/06070	06 September 2000	08 September 1999

TITLE OF INVENTION: REGISTER RENAMING SYSTEM

APPLICANT(S) FOR DO/EO/US: SEKI, Hajime

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [X] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information:
    - Executed small entity statement
    - Published Int'l. Appln. WO 01/18645 A1
    - English translation of Publ'd Int'l. Appln. No. WO 01/18645 A1

U.S. APPLICATION NO (if known, see 37 CFR 1.5) 10/069987	INTERNATIONAL APPLICATION NO PCT/JP00/06070	ATTORNEY'S DOCKET NUMBER 302-001

21. [X] The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	2 - 20 =		x **$18.00**	$	
Independent claims	2 - 3 =		x **$84.00**	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$	
TOTAL OF ABOVE CALCULATIONS =				$ 890	
[X] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. +				$ 445	
SUBTOTAL =				$ 445	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$	
TOTAL NATIONAL FEE =				$ 445	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
TOTAL FEES ENCLOSED =				$ 445	
				Amount to be refunded:	$
				charged:	$

a. [X] A check in the amount of $ 445.00 to cover the above fees is enclosed. (Check #16796)

b. [ ] Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 10-1213 . A duplicate copy of this sheet is enclosed.

d. [ ] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
Felix J. D'Ambrosio
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P.O. Box 2266 Eads Station
Arlington, VA 22202

SIGNATURE

Felix J. D'Ambrosio
NAME

25,721
REGISTRATION NUMBER

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
)
Hajime Seki)
)
Appln. No. : TBA)
)
Filed : March 8, 2002)
)
For : REGISTER RENAMING SYSTEM)

PRELIMINARY AMENDMENT

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to an examination on the merits, please amend this application as follows:

AMENDMENTS

IN THE SPECIFICATION:

Please amend page 3 as follows:

--present invention, a larger number of instructions could be processed per cycle owing to pipelining where dependency checks among instructions are to be done as a pre-process.

To begin with, in regard to a group of instructions that are to go through the process of register renaming simultaneously, the pre-process is done as follows.

(a) Each logical-register number shown as a destination operand is marked with a tag that corresponds to the order of the instruction. These tags are labels that, in the later stage, are to be replaced by physical-register numbers that are taken out of the free list and allocated.

(b) Each logical-register number shown as a source operand that is RAW (read-after-write) dependent on an instruction that goes through the process of register renaming simultaneously is marked with the same tag that is being marked on the destination operand of the instruction on which it is dependent.

After the above pre-process, the logical-register numbers shown as operands in the group of instructions are respectively renamed to appropriate physical-register numbers. Each logical-register number on which a tag is marked is renamed to the physical-register number that is to be taken out of the free list and allocated in correspondence with the marked tag. Each logical-register number on which no tag is marked is renamed to the physical-register number that is to be obtained by accessing the mapping table.

In the same cycle, the contents of the mapping table are updated. Namely, contents of entries of the mapping table that correspond--

Please amend page 6 as follows:

--the processor of this embodiment is furnished with four F registers F1, F2, F3, and F4.

The register file 28 in the FL, each entry of which is designed to hold a physical-register number, is utilized to construct a circular FIFO queue. Namely, the numbers of physical registers that are being released from allocation are to be enqueued, and physical-register numbers are to be supplemented from the head of the queue to F registers out of which physical-register numbers are being taken.

Described below is the process of register renaming in this embodiment.

In this embodiment, register renaming is carried out through two stages (1) pre-process, and (2) execution of register renaming and updating of the MT. The action in each stage

is described below.

(1) Pre-process

In regard to a group of instructions that are to go through the process of register renaming simultaneously, the pre-process is done as follows.

(1a) Logical-register numbers shown as destination operands are respectively marked with tags @1, @2,..., each corresponding to the order of instruction. In this embodiment, tags @1, @2, @3, @4 respectively correspond to F registers F1, F2, F3, F4 in the FL.

(1b) Each logical-register number shown as a source operand that is RAW (read-after-write) dependent on an instruction that goes through the process of register renaming simultaneously is marked with the same tag that is being marked on the destination operand of the--

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Amended) A register renaming system for a processor based on superscalar architecture capable of out-of-order execution, comprising:

physical registers, the number of which is greater than that of the logical registers prescribed by the architecture;

a free list that is designed to hold unallocated physical-register numbers; and

a mapping table having entries that are provided in respective correspondence with the logical registers and each designed to hold a physical-register number,

wherein, for a group of instructions that are to go through the process of

register renaming simultaneously, after:

(a) marking each logical-register number shown as a destination operand with a tag that corresponds to the order of the instruction; and

(b) marking each logical-register number shown as a source operand that is RAW (read-after-write) dependent on an instruction that goes through the process of register renaming simultaneously with the same tag that is being marked on the destination operand of said instruction,

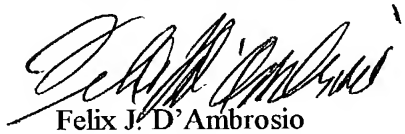
each logical-register number on which a tag is marked is renamed to the physical-register number that is to be taken out of said free list and allocated in correspondence with the marked tag; and

each logical-register number on which no tag is marked is renamed to the physical-register number that is to be obtained by accessing said mapping table.

REMARKS

The above amendments are intended to place this application in better condition for examination.

Respectfully submitted,



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MARKED-UP COPY OF PAGE 3 OF SPECIFICATION

--present invention, a larger number of instructions could be processed per cycle owing to pipelining where dependency checks among instructions are to be done as a pre-process.

To begin with, in regard to a group of instructions that are to go through the process of register renaming simultaneously, the pre-process is done as follows.

(a) Each logical-register number shown as a destination operand is marked with a tag that corresponds to the order of the instruction. These tags are labels that, in the later stage, are to be replaced by physical-register numbers that are taken out of the free list and allocated.

(b) Each logical-register number shown as a source operand that is RAW (read-after-write) [WAR (write-after-read)] dependent on an instruction that goes through the process of register renaming simultaneously is marked with the same tag that is being marked on the destination operand of the instruction on which it is dependent.

After the above pre-process, the logical-register numbers shown as operands in the group of instructions are respectively renamed to appropriate physical-register numbers. Each logical-register number on which a tag is marked is renamed to the physical-register number that is to be taken out of the free list and allocated in correspondence with the marked tag. Each logical-register number on which no tag is marked is renamed to the physical-register number that is to be obtained by accessing the mapping table.

In the same cycle, the contents of the mapping table are updated. Namely, contents of entries of the mapping table that correspond--

MARKED-UP COPY OF PAGE 6 OF SPECIFICATION

--the processor of this embodiment is furnished with four F registers F1, F2, F3, and F4.

The register file 28 in the FL, each entry of which is designed to hold a physical-register number, is utilized to construct a circular FIFO queue. Namely, the numbers of physical registers that are being released from allocation are to be enqueued, and physical-register numbers are to be supplemented from the head of the queue to F registers out of which physical-register numbers are being taken.

Described below is the process of register renaming in this embodiment.

In this embodiment, register renaming is carried out through two stages (1) pre-process, and (2) execution of register renaming and updating of the MT. The action in each stage is described below.

(1) Pre-process

In regard to a group of instructions that are to go through the process of register renaming simultaneously, the pre-process is done as follows.

(1a) Logical-register numbers shown as destination operands are respectively marked with tags @1, @2,..., each corresponding to the order of instruction. In this embodiment, tags @1, @2, @3, @4 respectively correspond to F registers F1, F2, F3, F4 in the FL.

(1b) Each logical-register number shown as a source operand that is [WAR (write-after-read)] RAW (read-after-write) dependent on an instruction that goes through the process of register renaming simultaneously is marked with the same tag that is being marked on the destination operand of the--

MARKED-UP COPY OF AMENDED CLAIM 1

1. (Amended) A register renaming system for a processor based on superscalar architecture capable of out-of-order execution, comprising:

physical registers, the number of which is greater than that of the logical registers prescribed by the architecture;

a free list that is designed to hold unallocated physical-register numbers; and

a mapping table having entries that are provided in respective correspondence with the logical registers and each designed to hold a physical-register number,

wherein, for a group of instructions that are to go through the process of register renaming simultaneously, after:

(a) marking each logical-register number shown as a destination operand with a tag that corresponds to the order of the instruction; and

(b) marking each logical-register number shown as a source operand that is [WAR (write-after-read)] RAW (read-after-write) dependent on an instruction that goes through the process of register renaming simultaneously with the same tag that is being marked on the destination operand of said instruction,

each logical-register number on which a tag is marked is renamed to the physical-register number that is to be taken out of said free list and allocated in correspondence with the marked tag; and

each logical-register number on which no tag is marked is renamed to the physical-register number that is to be obtained by accessing said mapping table.

SPECIFICATION

REGISTER RENAMING SYSTEM

FIELD OF THE INVENTION

The present invention relates to a register renaming system that can process a large number of instructions per clock cycle in a processor based on superscalar architecture capable of out-of-order execution.

DESCRIPTION OF THE PRIOR ART

A processor based on superscalar architecture capable of out-of-order execution is equipped with physical registers, the number of which is greater than that of the logical registers prescribed by the architecture. And the technique of dynamic register renaming is applied.

Namely, in each cycle, dependency checks are made by comparing the logical-register numbers shown as operands in the instructions, and the logical-register numbers are respectively renamed to appropriate physical-register numbers so that the dependencies would be dissolved.

For incarnation of register renaming, a technique utilizing a reorder buffer and a technique utilizing a mapping table are known. The technique utilizing a reorder buffer is adopted, for example, for the Pentium[tm] processor, available from Intel Corporation of Santa Clara, Calif. USA. The technique utilizing a mapping table is described in Keller, R. M. "Look-Ahead Processors." Computing Surveys, Vol. 7, no. 4 (December

1975), pp. 177-195, and is adopted, for example, for R10000[tm] processor, available from MIPS Technologies, Inc. of Mountain View, Calif. USA.

When compared with the technique utilizing a reorder buffer, the technique utilizing a mapping table should introduce one more pipeline stage to access the mapping table. But, the logical circuit for checking dependencies among instructions can be relatively simplified.

In regard to superscalar processors, it is desired to enhance performance by streamlining register renaming and decoding / issuing a larger number of instructions per cycle.

However, there has been a problem that it is difficult to increase the number of instructions that go through the process of register renaming per cycle beyond the current level, because it requires an extremely massive logical circuit.

The present invention has been proposed with a view to solving the foregoing problem. Its object is to provide a register renaming system whereby the number of instructions that can be processed per cycle could be increased beyond the current level.

SUMMARY OF THE INVENTION

The processor in which the register renaming system according to the present invention is incorporated comprises a free list that holds free, namely, unallocated physical-register numbers, and a mapping table whose entries are provided in respective correspondence with the logical registers and each designed to hold a physical-register number.

By means of the register renaming system according to the

present invention, a larger number of instructions could be processed per cycle owing to pipelining where dependency checks among instructions are to be done as a pre-process.

To begin with, in regard to a group of instructions that are to go through the process of register renaming simultaneously, the pre-process is done as follows.

(a) Each logical-register number shown as a destination operand is marked with a tag that corresponds to the order of the instruction. These tags are labels that, in the later stage, are to be replaced by physical-register numbers that are taken out of the free list and allocated.

(b) Each logical-register number shown as a source operand that is WAR (write-after-read) dependent on an instruction that goes through the process of register renaming simultaneously is marked with the same tag that is being marked on the destination operand of the instruction on which it is dependent.

After the above pre-process, the logical-register numbers shown as operands in the group of instructions are respectively renamed to appropriate physical-register numbers. Each logical-register number on which a tag is marked is renamed to the physical-register number that is to be taken out of the free list and allocated in correspondence with the marked tag. Each logical-register number on which no tag is marked is renamed to the physical-register number that is to be obtained by accessing the mapping table.

In the same cycle, the contents of the mapping table are updated. Namely, contents of entries of the mapping table that correspond

to logical-register numbers shown as destination operands in the group of instructions are respectively altered to physical-register numbers that are to be allocated in correspondence with the marked tags. In the case that the same logical-register number is shown as destination operand in a plurality of instructions, the alteration concerning the last in the order of instructions is validated.

As above, taking two stages, namely, by pipelining, it may be possible to have a larger number of instructions go through the process of register renaming per cycle with a relatively simple circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a piece of hardware that is needed for incarnation of the register renaming system according to the present invention; and

Fig. 2 shows contents of the mapping table and F registers, in the course of an example process of register renaming regarding a sequence of instructions in the embodiment of the present invention.

PREFERRED EMBODIMENTS OF THE INVENTION

In the following, a preferred embodiment that materializes the register renaming system according to the present invention will be described referring to the figures. Now, the later-described processor in which the register renaming system according to the present invention is incorporated is a RISC machine that is assumed to have 8 logical registers R0, R1, ... R7 on the architecture, furnished with 32 physical registers P00,

P01, ... P31 in hardware, and so structured as to be able to have up to four instructions go through the process of register renaming per cycle.

Fig. 1 is a block diagram of a piece of hardware that is needed for incarnation of the register renaming system according to the present invention. Shown in Fig. 1 are a mapping table 1 and a free list 2.

Described below is the detailed structure of each of the above-mentioned components.

(A) Mapping Table (MT)

As shown in Fig. 1, in this embodiment, the mapping table (hereafter, it will be referred to as the MT) 1 has eight entries 10 – 17 provided in respective correspondence with logical registers R0, R1, ... R7. Each MT entry is designed to hold a physical-register number.

(B) Free List (FL)

The free list (hereafter, it will be referred to as the FL) holds numbers of free, namely, unallocated physical registers.

In the case that a free physical register is to be allocated, a free physical-register number is taken out of the FL. Conversely, when a physical register is to be released from allocation, the number of the physical register gets to be registered on the FL.

As shown in Fig. 1, in this embodiment, FL 2 comprises F registers 21, 22, 23, 24 and a register file 28.

Each of the F registers is designed to hold a physical-register number. It is from F registers that free physical-register numbers are to be taken out of the FL. Namely, F registers are needed as many as instructions that go through the process of register renaming in a cycle. So,

the processor of this embodiment is furnished with four F registers F1, F2, F3, and F4.

The register file 28 in the FL, each entry of which is designed to hold a physical-register number, is utilized to construct a circular FIFO queue. Namely, the numbers of physical registers that are being released from allocation are to be enqueued, and physical-register numbers are to be supplemented from the head of the queue to F registers out of which physical-register numbers are being taken.

Described below is the process of register renaming in this embodiment.

In this embodiment, register renaming is carried out through two stages: (1) pre-process, and (2) execution of register renaming and updating of the MT. The action in each stage is described below.

(1) Pre-process

In regard to a group of instructions that are to go through the process of register renaming simultaneously, the pre-process is done as follows.

(1a) Logical-register numbers shown as destination operands are respectively marked with tags @1, @2, ..., each corresponding to the order of instruction. In this embodiment, tags @1, @2, @3, @4 respectively correspond to F registers F1, F2, F3, F4 in the FL.

(1b) Each logical-register number shown as a source operand that is WAR (write-after-read) dependent on an instruction that goes through the process of register renaming simultaneously is marked with the same tag that is being marked on the destination operand of the

instruction on which it is dependent. Namely, in regard to each of the instructions after the first one, each logical-register number shown as a source operand is compared with logical-register number(s) shown as destination operand(s) in the foregoing instruction(s). If matched, the same tag is marked on it. In the case that a plurality of matches come out, the tag concerning the last in the order of instructions is selected.

(2) Execution of Register Renaming and Updating of the MT

After the above-mentioned pre-process, the logical-register numbers shown as operands in the group of instructions are respectively renamed to appropriate physical-register numbers, and contents of the MT are updated. To put it in the concrete, the following process is carried out.

(2a) Each logical-register number on which a tag is marked is renamed to the physical-register number that is to be taken out of the FL and allocated in correspondence with the marked tag. Each logical-register number on which no tag is marked is renamed to the physical-register number that is to be obtained by accessing the MT.

(2b) Contents of MT entries that correspond to logical-register numbers shown as destination operands in the group of instructions are respectively altered to physical-register numbers that are to be allocated in correspondence with the marked tags. In the case that the same logical-register number is shown as destination operand in a plurality of instructions, the alteration concerning the last in the order of instructions is validated.

And, this concludes a general description of the process of register renaming in this embodiment. Next, an example action is

described below. Now, let's consider having the following four instructions go through the process of register renaming in the processor of this embodiment.

```
Instruction1   mul   R0, R1, R2      ; R0 = R1 * R2
Instruction2   mul   R1, R3, R4      ; R1 = R3 * R4
Instruction3   add   R0, R0, R1      ; R0 = R0 + R1
Instruction4   div   R0, R0, R5      ; R0 = R0 / R5
```

Assuming that registers R1, R2, R3, R4, R5 are to respectively hold data D1, D2, D3, D4, D5 according to the foregoing instructions, the above sequence of instructions is to compute {(D1*D2)+(D3*D4)}/D5 and store it into register R0.

In the following, the process of register renaming regarding the above sequence of instructions in the processor of this embodiment is described in detail.

To begin with, the pre-process for register renaming is done as follows.

```
Instruction1   mul   R0(@1), R1(none), R2(none)
Instruction2   mul   R1(@2), R3(none), R4(none)
Instruction3   add   R0(@3), R0(@1), R1(@2)
Instruction4   div   R0(@4), R0(@3), R5(none)
```

Namely, destination register operands, which are each shown right after the operation code in the instruction, are respectively marked with tags @1, @2, @3, @4 in order.

In regard to each of the instructions after the first one, each source register operand is compared with destination register operand(s) of

the foregoing instruction(s). If matched, the same tag is marked on it. In the case that a plurality of matches come out, the tag concerning the last in the order of instructions is selected.

In regard to Instruction1, no tag is marked on the source operands. But, in practice, a default tag (e.g. @0) may be marked on "no-tag-marked" source operands.

In regard to Instruction2, each source operand is compared with destination operand R0 of Instruction1. In this case, because no match comes out, no tag is marked on them.

In regard to Instruction3, each source operand is compared with the destination operands of Instruction1 and 2. In this case, because the 1st and 2nd source operand are matched with the destination operands of Instruction1 and 2 respectively, tags @1 and @2 are respectively marked on them.

In regard to Instruction4, each source operand is compared with the destination operands of Instruction1, 2 and 3. In this case, because the 1st source operand is matched with the destination operands of Instruction1 and 3, tag @3, which corresponds to the latter – Instruction3 –, is marked on it.

By implementing an appropriate circuit, the pre-process for register renaming such as above is performed in a cycle.

In the next cycle, execution of register renaming and updating of the MT are performed. Now, let's suppose that contents of the MT and F registers in the FL at this moment are as shown in Fig. 2(A).

Each register operand on which a tag is marked is renamed

to the physical-register number that is taken out of the FL and allocated in correspondence with the marked tag. And, each register operand on which no tag is marked is renamed to the physical-register number that is obtained by accessing the MT by the logical-register number. Then, the given sequence of instructions is converted into the following.

Instruction1 mul P19, P03, P22

Instruction2 mul P08, P29, P05

Instruction3 add P27, P19, P08

Instruction4 div P21, P27, P07

Besides, contents of the MT entries that correspond to destination operands of Instruction1-4 are respectively altered to physical-register numbers that are allocated in correspondence with the marked tags. Hereupon, as shown in Fig. 2(B), contents of the MT entries that correspond to R0 and R1 are altered to P21 and P08 respectively. As to R0, P19, P27 and P21 are allocated triply, and the last one – P21 – is written into the MT. Moreover, as shown in Fig. 2(B), free physical-register numbers P31, P01, P17, P14 are respectively supplemented to the F registers, out of which physical-register numbers have been taken out.

And, this concludes the process of register renaming regarding the given sequence of instructions in the processor of this embodiment.

Besides, the system might be so structured that the correspondence between logical-register numbers and tags regarding updating of the mapping table is determined in the pre-process stage.

Namely, in the case that the same logical-register number is shown as destination operand in a plurality of instructions that go through the process of register renaming simultaneously, each of said plurality of instructions except the last one is invalidated in regard to updating of the mapping table in the pre-process stage.

For example, the following determination is made in the pre-process stage in regard to the above-mentioned example action.

Instruction1 R0 → @1 : invalid

Instruction2 R1 → @2 : valid

Instruction3 R0 → @3 : invalid

Instruction4 R0 → @4 : valid

And, in the next cycle, for each validated alteration, writing of the physical-register number allocated in correspondence with the marked tag is enabled.

As above, by also introducing a pre-process regarding updating of the mapping table, further simplification of the circuit may be attained.

INDUSTRIAL UTILITY

As above, by means of the register renaming system of the present invention, owing to pipelining where dependency checks among instructions are to be done as a pre-process, it may be possible to process a larger number of instructions per cycle with a relatively simple circuit.

WHAT IS CLAIMED IS:

1. A register renaming system for a processor based on superscalar architecture capable of out-of-order execution, comprising:

physical registers, the number of which is greater than that of the logical registers prescribed by the architecture;

a free list that is designed to hold unallocated physical-register numbers; and

a mapping table having entries that are provided in respective correspondence with the logical registers and each designed to hold a physical-register number,

wherein, for a group of instructions that are to go through the process of register renaming simultaneously, after:

(a) marking each logical-register number shown as a destination operand with a tag that corresponds to the order of the instruction; and

(b) marking each logical-register number shown as a source operand that is WAR (write-after-read) dependent on an instruction that goes through the process of register renaming simultaneously with the same tag that is being marked on the destination operand of said instruction,

each logical-register number on which a tag is marked is renamed to the physical-register number that is to be taken out of said free list and allocated in correspondence with the marked tag; and

each logical-register number on which no tag is marked is renamed to the physical-register number that is to be obtained by accessing said mapping table.

2. A free list comprising:

F registers, to the number of instructions that can go through the process of register renaming in a clock cycle, each of which is designed to hold a physical-register number; and

a circular FIFO queue that is made of a register file each entry of which is designed to hold a physical-register number,

wherein physical-register numbers that are being released from allocation are to be entered into said queue; and

physical-register numbers are to be supplemented from the head of said queue to F registers out of which physical-register numbers are being taken.

ABSTRACT

A register renaming system for a processor based on superscalar architecture that can process a larger number of instructions per cycle by providing a free list to hold unallocated physical-register numbers and a mapping table whose entries are provided in respective correspondence with the logical registers and each designed to hold a physical-register number, and by pipelining where dependency checks among instructions are to be done as a pre-process.

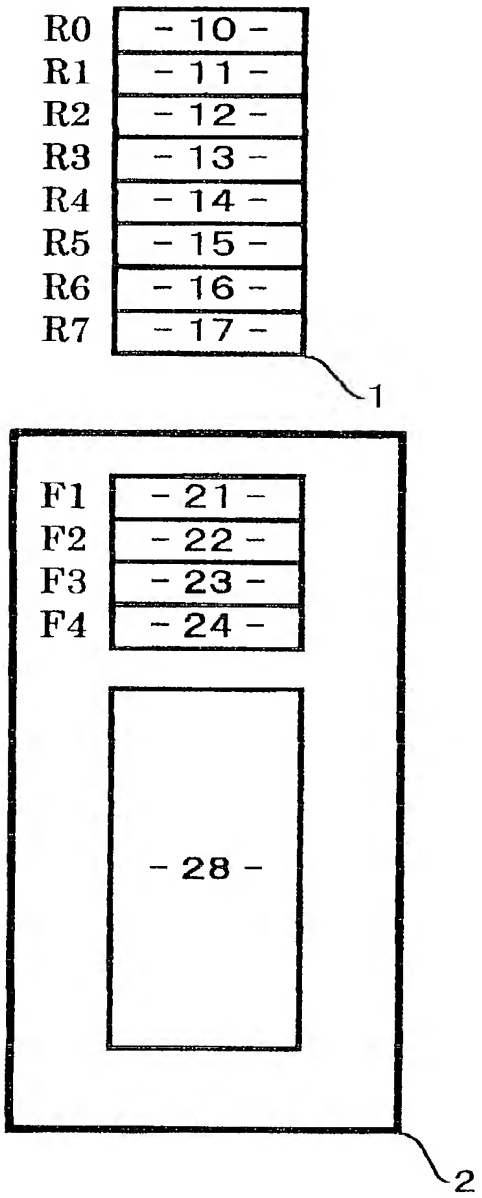
R0
R1
R2
R3
R4
R5
R6
R7
- 10 -
- 11 -
- 12 -
- 13 -
- 14 -
- 15 -
- 16 -
- 17 -
1
F1
F2
F3
F4
- 21 -
- 22 -
- 23 -
- 24 -
- 28 -
2

Fig.1

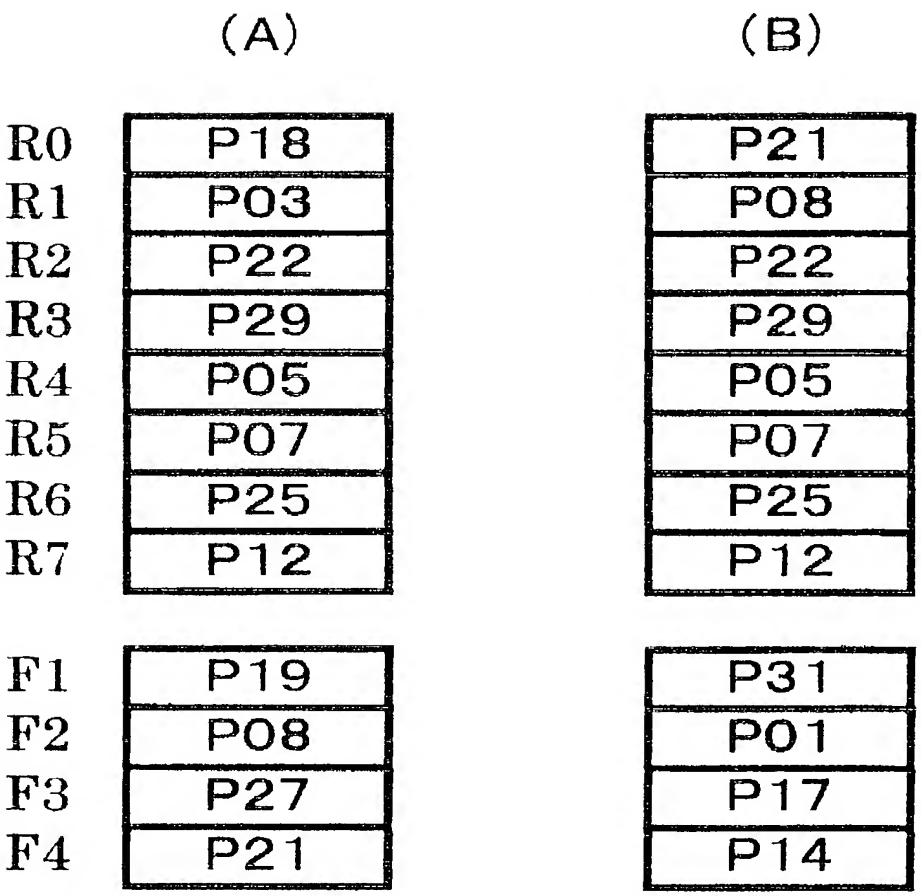
(A)
(B)
R0
R1
R2
R3
R4
R5
R6
R7
P18
P03
P22
P29
P05
P07
P25
P12
P21
P08
P22
P29
P05
P07
P25
P12
F1
F2
F3
F4
P19
P08
P27
P21
P31
P01
P17
P14

Fig.2

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:
This declaration is of the following type:

[ ] original
[ ] design
[ ] supplemental
[x] national stage of PCT
[ ] divisional
[ ] continuation
[ ] continuation-in-part (CIP)

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed for and for which a patent is sought on the invention entitled:

REGISTER RENAMING SYSTEM

the specification of which

[x] is attached hereto
[ ] was filed on _____,as
Application Serial No._____
and was amended on _____
(if applicable)
[x] was described and claimed in PCT International application
No. PCT/JP00/06070 filed on 6 September 2000
and as amended under PCT Article 19 on _____
(if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any Amendment referred to above.

I acknowledge duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56.

[ ] In compliance with this duty there is attached an information disclosure statement. 37 CFR 1.97.
I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent of inventor's certificate having a filing

dated before that of the application on which priority is claimed:

[ ] no such applications have been filed
[x] such application have been filed as follows.

Prior Foreign Application(s)

11-254149	Japan	8 September 1999	[x]	[ ]
(Number)	(Country)	(day-month-year filed)	Yes	No
			[ ]	[ ]
(Number)	(Country)	(day-month-year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Sec. 120 of any United States application(s) listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose all information known to be material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or

imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00

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Applicant or Patentee: Hajime Séki Attorney's
Serial or Patent No.: Docket No.:
Filed or Issued:
For: Register Renaming System

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9 (f) and 1.27 (b)) — INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9 (c) for purposes of paying reduced fees under section 41 (a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled Register Renaming System described in

[X] the specification filed herewith
[ ] application serial no. , filed .
[ ] patent no. , issued .

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9 (c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9 (d) or a nonprofit organization under 37 CFR 1.9 (e).

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[X] no such person, concern, or organization
[ ] persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

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ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28 (b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Hajime Seki
NAME OF INVENTOR NAME OF INVENTOR NAME OF INVENTOR

Hajime Seki
Signature of Inventor Signature of Inventor Signature of Inventor

Mar. 1, 2002
Date Date Date